What is claimed is:

1. A receiver comprising:

a first inverter comprising an input port having an input voltage and an output port;

a pFET comprising a gate connected to the input port and a drain connected to the output port; and

a nFET comprising a gate connected to the input port and a drain connected to the output port;

wherein the receiver has a first inversion threshold for the input voltage transitioning from HIGH to LOW, and a second inversion threshold for the input voltage transitioning from LOW to HIGH, where the first inversion threshold is greater than the second inversion threshold.

2. The receiver as set forth in claim 1, further comprising:

a pullup pFET comprising a gate and a drain connected to the source of the pFET; and

a pulldown nFET comprising a gate connected to the gate of the pullup pFET and a drain connected to the source of the nFET.

3. The receiver as set forth in claim 1, further comprising a second inverter to couple the input port to the gates of the pullup pFET and the pulldown nFET.

4. The receiver as set forth in claim 3, wherein the second inverter is a symmetrical inverter.

5. The receiver as set forth in claim 3, wherein the second inverter comprises an input port, wherein the second inverter has a first inversion threshold when there is a voltage at its input port transitioning from HIGH to LOW and has a second inversion threshold when the voltage at its input port is transitioning from LOW to HIGH, wherein the first inversion threshold is less than the second inversion threshold.

6. A receiver comprising:

a first inverter comprising an input port and an output port;

a HIGH power rail;

a LOW power rail;

a pFET comprising a gate coupled to the input port, a drain coupled to the output port, and a source; and

a nFET comprising a gate coupled to the input port, a drain coupled to the output port, and a source;

wherein when the input port is undergoing a voltage transition from HIGH to LOW, there is a low impedance path between the source of the pFET and the HIGH rail and no low impedance path between the source of the nFET and the LOW rail; and

wherein when the input port is undergoing a voltage transition from LOW to HIGH, there is no low impedance path between the source of the pFET and the HIGH rail and a low impedance path between the source of the nFET and the LOW rail.

7. The receiver as set forth in claim 6, further comprising:

a pullup pFET to provide the low impedance path between the source of the pFET and the HIGH rail when the input port is undergoing a voltage transition from HIGH to LOW; and

a pulldown nFET to provide the low impedance path between the source of the nFET and the LOW rail when the input port is undergoing a voltage transition from LOW to HIGH.

8. The receiver as set forth in claim 7, wherein the pullup pFET comprises a gate and the pulldown nFET comprises a gate, the receiver further comprising:

a second inverter to couple the input port to the gates of the pullup pFET and the pulldown nFET.

9. The receiver as set forth in claim 8, wherein the second inverter is a symmetrical inverter.

10. The receiver as set forth in claim 8, wherein the second inverter comprises an input port, wherein the second inverter has a first inversion threshold when there is a voltage at its input port transitioning from HIGH to LOW and has a second inversion threshold when the voltage at its input port is transitioning from LOW to HIGH, wherein the first inversion threshold is less than the second inversion threshold.

11. A receiver comprising:

a first inverter comprising an input port and an output port;

a pFET comprising a gate connected to the input port, a drain connected to the output port, and a source;

a nFET comprising a gate connected to the input port, a drain connected to the output port, and a source;

a pullup pFET comprising a gate and a drain connected to the source of the pFET;

a pulldown nFET comprising a gate and a drain connected to the source of the nFET; and

a second inverter coupling the input port to the gates of the pulldown nFET and the pullup pFET.

12. The receiver as set forth in claim 11, wherein the second inverter is a symmetrical inverter.

13. The receiver as set forth in claim 11, wherein the second inverter comprises an input port, wherein the second inverter has a first inversion threshold when there is a voltage at its input port transitioning from HIGH to LOW and has a second inversion threshold when the voltage at its input port is transitioning from LOW to HIGH, wherein the first inversion threshold is less than the second inversion threshold.

14.. A receiver comprising:

a first inverter comprising an input port having an input voltage and an output port;

a pFET comprising a gate and a drain connected to the output port;

a nFET comprising a gate and a drain connected to the output port;

a first transmission gate to couple the gate of the pFET to the input port; and

a second transmission gate to couple the gate of the nFET to the input port;

wherein the receiver has a first inversion threshold for the input voltage transitioning from HIGH to LOW, and a second inversion threshold for the input voltage transitioning from LOW to HIGH, where the first inversion threshold is greater than the second inversion threshold.

15. The receiver as set forth in claim 14, further comprising a second inverter to couple the first and second transmission gates to the input port.

16. The receiver as set forth in claim 15, wherein the second inverter is a symmetrical inverter.

17. The receiver as set forth in claim 15, wherein the second inverter comprises an input port, wherein the second inverter has a first inversion threshold when there is a voltage at its input port transitioning from HIGH to LOW and has a second inversion threshold when the voltage at its input port is transitioning from LOW to HIGH, wherein the first inversion threshold is less than the second inversion threshold.

18. A receiver comprising:

a first inverter comprising an input port having an input voltage and an output port;

a pFET comprising a gate and a drain connected to the output port;

a nFET comprising a gate and a drain connected to the output port;

a first transmission gate;

a second transmission gate; and

wherein when the input voltage is transitioning from HIGH to LOW, the first transmission gate is ON to provide a low impedance path between the gate of the pFET and the input port, and the second transmission gate is OFF to provide a high impedance path between the gate of the nFET and the input port; and when the input voltage is transitioning from LOW to HIGH, the second transmission gate is ON to provide a low impedance path between the gate of the nFET and the input port, and the first transmission gate is OFF to provide a high impedance path between the gate of the pFET and the input port.

19. The receiver as set forth in claim 18, further comprising:

a pullup pFET comprising a drain connected to the gate of the pFET to keep the pFET OFF when the first transmission gate is OFF; and

a pulldown nFET comprising a drain connected to the gate of the nFET to keep the nFET OFF when the second transmission gate is OFF.

20. The receiver as set forth in claim 19, further comprising:

a second inverter to couple the first transmission gate, the second transmission gate, the pullup pFET, and the pulldown nFET to the input port.

21. The receiver as set forth in claim 20, wherein the second inverter is a symmetrical inverter.

22. The receiver as set forth in claim 20, wherein the second inverter comprises an input port, wherein the second inverter has a first inversion threshold when there is a voltage at its input port transitioning from HIGH to LOW and has a second inversion threshold when the voltage at its input port is transitioning from LOW to HIGH, wherein the first inversion threshold is less than the second inversion threshold.

23. The receiver as set forth in claim 18, further comprising:

a second inverter to couple the first transmission gate and the second transmission gate to the input port.

24. The receiver as set forth in claim 23, wherein the second inverter is a symmetrical inverter.

25. The receiver as set forth in claim 23, wherein the second inverter comprises an input port, wherein the second inverter has a first inversion threshold when there is a voltage at its input port transitioning from HIGH to LOW and has a second inversion

threshold when the voltage at its input port is transitioning from LOW to HIGH, wherein the first inversion threshold is less than the second inversion threshold.

26. A computer system comprising:

memory;

a die in communication with the memory, the memory not residing on the die, the die comprising a receiver, the receiver comprising:

a first inverter comprising an input port having an input voltage and an output port;

a pFET comprising a gate connected to the input port and a drain connected to the output port; and

a nFET comprising a gate connected to the input port and a drain connected to the output port;

wherein the receiver has a first inversion threshold for the input voltage transitioning from HIGH to LOW, and a second inversion threshold for the input voltage transitioning from LOW to HIGH, where the first inversion threshold is greater than the second inversion threshold.

27. A computer system comprising:

memory;

a die in communication with the memory, the memory not residing on the die, the die comprising a receiver, the receiver comprising:

a first inverter comprising an input port having an input voltage and an output port;

a pFET comprising a gate and a drain connected to the output port;

a nFET comprising a gate and a drain connected to the output port;

a first transmission gate to couple the gate of the pFET to the input port; and

a second transmission gate to couple the gate of the nFET to the input port;

wherein the receiver has a first inversion threshold for the input voltage transitioning from HIGH to LOW, and a second inversion threshold for the input voltage transitioning from LOW to HIGH, where the first inversion threshold is greater than the second inversion threshold.